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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/728,301	12/01/2000	Roubik Gregorian	10262-01400US	4922

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Paul C. Haughey
TOWNSEND and TOWNSEND and CREW LLP
8th Floor
Two Embarcadero Center
San Francisco, CA 94111-3834

EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/728,301	GREGORIAN ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendments filed on 3/29/04 in which claims 1-13 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection therefore this case is made final.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyue U.S. Patent No 6,359,936 B1 in view of Oi U.S. Patent No 6,434,220 B2.

As per claim 1, Shyue teaches a digital line build out circuit comprising: a memory storing a plurality of digitized waveforms (see figs. 4-6, 8a-8b elements 80 or 100 and col.2, lines 5-6 and col.6, lines 65-67 and col.7, lines 1-20); a selection circuit, coupled to said memory, to select (see figs.4-6, 8a-8b elements 74, 184, 200, 284 and col.9, lines 10-25 and col.10, lines 43-67) certain ones of said waveforms corresponding to an anticipated amount of signal degradation over a transmission line; and a digital to analog converter (see element 44 and col.7, lines 13-20) to convert said certain ones of said waveforms into analog waveforms for transmission.

However Shyue does not teach selected said waveforms over a wired transmission line.

Oi teaches selected said waveforms over a wired transmission line (see col.8, lines 60-65 and col.9, lines 13-30).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Oi into Shyue so that the transmission signal could be propagated through the metallic subscriber line having an extended distance with a reduced deterioration as taught by Oi (see col.9, lines 1-2).

As per claim 2, Shyue does include a counter (see fig.4 element 54) having an output coupled to inputs of said memory for sequentially selecting multiple samples of said digitized waveforms during a period.

As per claim 3, Shyue does include said memory comprises a ROM (fig.5 element 80).

As per claims 4 and 7, Shyue does include an adder or summer is the same as the claimed (a combining circuit) (see fig.7 element 290 and col.9, lines 37-40), coupled between said memory and said digital to analog converter, to combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform.

As per claim 8, Shyue teaches a digital line build out circuit comprising: a memory storing a plurality of digitized waveforms (see figs. 4-6, 8a-8b elements 80 or 100 and col.2, lines 5-6 and col.6, lines 65-67 and col.7, lines 1-20); a selection circuit, coupled to said memory select (see figs.4-6, 8a-8b elements 74, 184, 200, 284 and col.9, lines 10-25 and col.10, lines 43-67), to select certain ones of said waveforms corresponding to an anticipated amount of signal degradation over a transmission line; a digital to analog converter (see element 44 and col.7, lines 13-20) to convert said certain ones of said waveforms into analog waveforms for transmission; a counter (see figs 4-6, 8a-8b element 54) having an output coupled to inputs of said memory for sequentially

selecting multiple samples of said digitized waveforms during a period; an adder or summer is the same as the claimed (a combining circuit) (see fig.7 element 290 and col.9, lines 37-40), coupled between said memory and said digital to analog converter, to combine a portion of a current digitized waveform with a portion of at least one previous digitized waveform.

However Shyue does not teach selected said waveforms over a wired transmission line.

Oi teaches selected said waveforms over a wired transmission line (see col.8, lines 60-65 and col.9, lines 13-30).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Oi into Shyue so that the transmission signal could be propagated through the metallic subscriber line having an extended distance with a reduced deterioration as taught by Oi (see col.9, lines 1-2).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-6 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyue U.S. Patent NO 6,359,936 B1 in view of Oi U.S. Patent No 6,434,220 B2 and in further view of Sung U.S. Patent No 5,808,688.

As per claim 5, Shyue and Oi in combination disclose all the features of the claimed invention except said combining circuit includes at least one delay element for delaying an output of said memory for said previous digitized waveform for combination with said current digitized waveform.

Sung teaches combining circuit includes at least one delay element for delaying (see fig.3a elements D1-D7 and col.4, lines 39-67) an output of said memory for said previous digitized waveform for combination with said current digitized waveform.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Sung into Shyue and Oi as to perform interpolation in order to provide a high quality picture during format conversion as taught by Sung (see col.2, lines 5-7)

As per claim 6, Sung teaches delay element delays a data bit, and further comprising a multipliers is considered as the claimed (circuit for gating) (see fig. 3a elements 361-372 and col.4, lines 47-67) a portion of said digitized waveform from said memory based on a value of said data bit. Therefore implementing the teaching of Sung into Shyue would have been obvious to one skilled in the art as to perform interpolation in order to provide a high quality picture during format conversion as taught by Sung (see col.2, lines 5-7).

As per claim 9, Shyue teaches a digital line build out circuit comprising: a memory storing a plurality of digitized waveforms (see figs. 4-6, 8a-8b elements 80 or 100 and col.2, lines 5-6 and col.6, lines 65-67 and col.7, lines 1-20) corresponding to different anticipated amounts of signal degradation over a transmission line, each of said digitized waveforms having a plurality of separately addressable portions; a an adder or summer is the same as the claimed (a combining circuit) (see fig.7 element 290 and col.9,

lines 37-40) having inputs coupled to outputs of switching circuits (see fig.7 element 288) for combining multiple ones of said separately addressable portions; a digital to analog converter (see element 44 and col.7, lines 13-20) coupled to an output of said combining circuit; a shift register is the same as the claimed (configuration input) (see fig.6 element 58 and col.9, lines 3-5), coupled to said memory, for selecting a desired one of said plurality of digitized waveforms; and a counter (see figs 4-6, 8a-8b element 54), coupled to said memory, for sequentially selecting a plurality of digitized values for said separately addressable portions.

However Shyue does not teach a data line coupled to a plurality of serial delay elements; a plurality of gating circuits having a first input coupled to one of said data line and an output of each of said delay elements, and a second input coupled to an output of said memory for one of said separately addressable portions; a combining circuit having inputs coupled to outputs of said gating circuits for combining multiple ones of said separately addressable portions.

Sung teaches a data line coupled a plurality of serial delay elements (see fig.3a elements D1-D7 and col.4, lines 39-67); a plurality of multipliers is considered as the claimed (gating circuits) (see fig.3a elements 361-373 and col.4, lines 46-67) having a first input coupled to one of said data line and an output of each of said delay elements, and a second input coupled to an output of said memory (see fig.3a element 35) for one of said separately addressable portions; a an adder or summer is the same as the claimed (a combining circuit) (see fig.3a elements 365, 375 and col.4, lines 49-67 and col.9, lines 37-40) having inputs coupled to outputs of said gating circuits for combining multiple ones of said separately addressable portions.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Sung into Shyue as to perform interpolation in order to provide a high quality picture during format conversion as taught by Sung (see col.2, lines 5-7)

As per claims 10 and 11, Shyue does teach said memory is a ROM (see fig.5 element 80) having a plurality of memories.

As per claim 12, Sung teaches a multiplier circuits. Therefore implementing the teaching of Sung into Shyue would have been obvious to one skilled in the art as to perform interpolation in order to provide a high quality picture during format conversion as taught by Sung (see col.2, lines 5-7).

As per claim 13 Shyue does teach a selector circuits (see fig.8b element 284).

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Leveque U.S. Patent No 5,495,468 teaches a system and method for transmitting plural information waveforms.

Kochan U.S. Patent No 6,195,614B1 teaches a method of characterizing events.

Leveque U.S. Patent No 5,454,010 teaches a system and method for calibration of frequency hopping.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is (703) 308-9573. The examiner can normally be reached on Monday-Thursday from 8:00 AM - 5:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour, can be reached on (703) 306-3034. The fax phone number for this Group is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Emmanuel Bayard

Primary Examiner

6/5/04

EMMANUEL BAYARD
PRIMARY EXAMINER